In the Specification:

Please replace the paragraph beginning on page 1, line 16 with the following:

First, in order to solve the eigenvalue problem of a real symmetric matrix (matrix composed of real numbers, which does not ~~changed~~ change even if the matrix elements are transposed) and an Hermitian matrix (matrix composed of complex numbers, which does not ~~changed~~ change even if conjugated and transposed)(calculating λ, in which $\det|A-\lambda I| = 0$, and the eigenvector thereof if a matrix, a constant and a unit matrix are assumed to be A, λ and I, respectively), tri-diagonalization (conversion into a matrix with a diagonal factor and adjacent factors on both sides only) has been applied. Then, the eigenvalue problem of this tri-diagonal matrix is solved using a multi-section method. The eigenvalue is calculated and the eigenvector is calculated using an inverse repetition method. Then, Householder conversion is applied to the eigenvector, and the eigenvector of the original eigenvalue problem is calculated.

Please replace the paragraph beginning on page 7, line 7 with the following:

In the preferred embodiment of the present invention, conventional methods are used to calculate an eigenvalue based on a tri-diagonalized matrix and to calculate the eigenvector of the tri-diagonalized matrix~~,~~.

Please replace the paragraph beginning on page 7, line 7 with the following:

Each of processors 10-1 through 10-n has primary cache memory, and this primary cache memory is sometimes built into each processor. Each of the processors 10-1 through 10-n is also provided with each of secondary cache memories 13-1 through 13-n, and each of the secondary cache memories 13-1 through 13-n is connected to an interconnection network 12. The interconnection network 12 is also provided with memory modules 11-1 through 11-n, which are shared memories. Each of the processors 10-1 through 10-n reads necessary data from one of the memory modules, stores the data in one of the secondary cache memories 13-1 through 13-n or one of the primary cache memories through the interconnection network 12, and performs ~~calculation~~ calculations.

Please replace the paragraph beginning on page 8, line 4 with the following:

In this case, the speed of reading data from one of the memory ~~module~~ modules 11-1 through 11-n into one of the secondary cache memories 13-1 through 13-n or one of the primary cache memories and the speed of writing calculated data into one of the memory modules 11-1 through 11-n from one of the primary cache memories is very low compared with the calculation speed of each of the processors 10-1 through 10-n. Therefore, the frequent occurrence of such reading or writing degrades the performance of the entire computer.

Please replace the paragraph beginning on page 8, line 4 with the following:

In order to tri-diagonalize each block, the following vectors used for Householder conversion must be updated. In order to localize these calculations as much as possible, a submatrix of the given block width must be copied into a work area, and is tri-diagonalized and ~~is~~ stored in the original area. Instead of updating a subsequent column vector for each calculation, calculation is performed in the form of a matrix product with improved calculation density. Therefore, the tri-diagonalization of each block is performed by a recursive program.

Please replace the paragraph beginning on page 13, line 11 with the following:

The calculation of Fig. 4B is performed after the calculation of Fig. 4A, the calculation of Fig. 4D is performed after the calculation of ~~Fig. C~~ Fig. 4C and the calculation of Fig. 4F is performed after the calculation of Fig. 4E.

Please replace the paragraph beginning on page 16, line 18 with the following:

Then, the calculated result is copied into the upper half. Similarly, this is also divided and the load is balanced. In this case, portions other than the diagonal block are divided into fairly small blocks so that data are not read across a plurality of pages of cache memory and are copied. The lower triangular matrix is updated by $A_{n+k}=A_n-U_kW_k^t-W_kU_k^t$. In this case, the lower triangular matrix is divided into #CPU×2 of column blocks, two outermost blocks, one at each end are sequentially paired. Each CPU updates such a pair. Fig. 7 shows a case where four CPUs are provided.

Please replace the paragraph beginning on page 43, line 18 with the following:

For basic algorithms of matrix computations, see the following textbook:

G.H.Golub and C.F.Van Loan, "Matrix ~~Computatrions~~ Computations" the third edition, The Johns Hopkins University Press (1996).